Facing the Challenge of ESD Control for Ultra-Sensitive (Class 0) Devices

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Abstract

Successful high-yield production and handling of ESD-sensitive devices has been the result two mostly separate endeavors: 1. The development of electrostatic *control* methods and their implementation into manufacturing processes and 2. The design and fabrication of special ESD *protection* circuits to improve device ESD robustness. However, very few of the protection strategies in place today would be successful without a minimum level of controls. So, over the last several decades there has been a tenuous balance between control and protection. However, current technology trends tell us that in the near future this balance is threatened. In this seminar, we discuss how the implementation of basic techniques for ESD control must change with evolving technology and inevitable lowering of device thresholds, especially for Charged Device Model (CDM). Electrostatic parameters that should be considered for monitoring production and handling of ultra-sensitive electronic products will be presented. The ESD Technology Roadmap will also be reviewed and enhancements needed for high-reliability will be discussed. We will also discuss how device-level ESD stress test methods have helped provide a practical but imperfect link between ESD control and protection. The discussion will include some case histories that exposed mismatches in the balance between control and protection.